REMARKS

Claims 1-31 are pending in the application. Claims 1-31 are rejected. Claims 1, 14, and 23 have been amended and a marked-up version illustrating the claim amendments is annexed hereto.

Claim Rejections- 35 U.S.C. § 103(a)

Claims 1-31 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Singh et al. (U.S. Patent 6,042,687) in view of DeOrnellas et al. (U.S. Patent 6,046,116) and further in view of Yang (U.S. Patent 5,827,437) and Muller et al. (U.S. Patent 5,605,600).

It is respectfully submitted that at the very minimum the combination of Singh, DeOrnellas, Yang, and Muller is legally deficient to establish a prima facie case of obviousness under 35 U.S.C. §103(a) to support the rejection of claims 1, 14, and 23 because the combination does not teach or suggest *etching deep trenches in a silicon substrate...wherein the deep trenches have a depth of about 8um or greater and wherein the deep trench etching is performed for a ground rule design of 175nm or less,* as essentially claimed in claims 1, 14, and 23.

Advantageously, the methods of claims 1, 14, and 23 enable the formation of deep trenches having depths that are not obtainable using conventional deep trench etching methods due to the accumulation and re-deposition of etch by-products that cause, *inter alia,* trench "pinch-off" and impedes the formation of a deep trench, especially for 175nm ground rules and below.

The Examiner acknowledges that neither Singh, DeOrnellas, nor Yang teach a method for etching deep trenches in a substrate that have an etching depth of about 7um or greater.

Applicants respectfully submit that Muller does not cure the deficiencies of Singh, DeOrnellas, or Yang because Muller does not disclose or suggest *etching deep trenches in a silicon substrate...wherein the deep trenches have a depth of about 8um or greater and wherein the deep trench etching is performed for a ground rule design of 175nm or less.*

Further, Applicants respectfully submit that at the very minimum, one of ordinary skill in the art would not be motivated to combine Muller with Singh, DeOrnellas, and Yang to derive the claimed inventions. Although Muller discloses etching trenches while heating the wafer to about 130°C (see FIG. 3), the claimed invention includes heating the wafer to temperatures of above 200 degrees Celsius which, as explained in Applicants' disclosure, eliminates the re-depositing of etch by-products from accumulating at the top of the deep trench to prevent trench "pinch-off." Muller does not address these problems.

Therefore, claims 1, 14, and 23 are believed to be patentable and non-obvious over the combination of Singh, DeOrnellas, Yang, and Muller. Further, all pending claims that depend from claims 1, 14, and 23 are believed to be non-obvious and patentable over such combination at least for the reasons given above for respective base claims 1, 14, and 23.

Accordingly, the withdrawal of the rejections under 35 U.S.C. § 103(a) is respectfully requested.

In view of the foregoing remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

Respectfully submitted,

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IN THE CLAIMS (Marked-up Version):

1. (Thrice Amended) A method for etching deep trenches in a substrate, comprising the steps of:

securing a wafer to an electrode in a plasma chamber, the wafer comprising a silicon substrate;

heating the wafer to a temperature of greater than 200 degrees Celsius; and

exposing the wafer to a reactive plasma to etch deep trenches into the silicon substrate of the wafer, wherein the deep trenches have a depth of about [7um] 8um or greater and wherein the deep trench etching is performed for a ground rule design of 175nm or less.

14. (Thrice Amended) A method for etching deep trenches in a substrate, comprising the steps of;

forming a hardmask on a silicon substrate of a wafer;

patterning the hardmask;

securing the wafer to an electrode in a plasma chamber;

maintaining the electrode at a temperature of between about 200 and about 450 degrees Celsius to achieve about the same temperature in the wafer; and

exposing the wafer to a reactive plasma to etch deep trenches into the silicon substrate of the wafer in accordance with the hardmask pattern, wherein the deep trenches have a depth of about [7um] 8um or greater and wherein the deep trench etching is performed for a ground rule design of 175nm or less.

23. (Thrice Amended) A method for etching deep trenches in a substrate, comprising the steps of:

clamping a wafer onto a electrode in a plasma chamber, the wafer comprising a silicon substrate;

maintaining the electrode at an elevated temperature between of about 200

degrees and 450 degrees Celsius;

exposing the wafer to a reactive plasma including Cl_2, BCL_3, Ar, O_2, and N_2;

applying a backside pressure to the clamped wafer using He to achieve thermal contact between the wafer and the electrode such that the wafer is maintained at about the same temperature as the electrode; and

applying a bias power to the wafer electrode to accelerate ions from the plasma to achieve etching of the silicon substrate to form deep trenches, wherein the deep trenches have a depth of about [7um] 8um or greater and wherein the deep trench etching is performed for a ground rule design of 175nm or less.